WAVER LEVEL PACKAGING
Product Overview

Industry Landscape

Semiconductor wafer level packaging (WLP) continues to grow. Drivers for WLP growth include mobility with more memory, IoT, Sensors, wearables, automotive, LED and other demanding applications. Products in these markets are required to be smaller, perform better, cost less and last longer. This growth is driven by shrinking wafer nodes, smaller footprints, increased electrical performance and thermal conductivity requirements.

WLP chemistry is a critical component in helping wafer foundries, OEMs and IDMs address the ever-changing industry landscape. In this “advanced packaging world,” there are fewer and fewer off-the-shelf solutions. WLP designs require specific electroplated copper features to support interconnect integration schemes.

Merchant and captive bumping operations are shifting from conventional chemistries that traditionally supported a variety of electroplated features that are formulated to meet specific designs, applications and tools. The development of next generation process chemistry requires close collaboration across the entire industry.

Value Creation

MacDermid Alpha is uniquely positioned to support the integration between front-end wafer fabrication and back-end assembly processes including redistribution Layer (RDL), Wafer Bumping, Pillar and Through Silicon Via (TSV) fill. Also available are gold products used in compound semiconductor market.

As a technology company committed to addressing current and emerging application requirements, we provide chemistries optimized to meet your specific design and tool capabilities.

By establishing strategic partnerships with leading equipment and material suppliers, we continuously co-develop advanced chemistries demanded by today’s highly competitive semiconductor market. This collaborative model enables us to accelerate product development for shortest time to market, while also meeting environmental, health and safety concerns that align with your company’s technology roadmaps.
Applications Expertise

MacDermid Enthone WLP Applications Laboratories are strategically located to support some of the world’s leading semiconductor manufacturers. Whether it is with new or emerging technologies, we assist our customers as they advance their product portfolio and implement higher performance, cost-effective wafer manufacturing at their facilities throughout the globe.

Our laboratories are staffed by highly trained applications engineers and R&D chemists who assist our customers in process optimization, troubleshooting, and bath analysis. Outfitted with the latest technology in materials analysis, we routinely assist customer projects with characterization of plated features and deposits for bump height, morphology, alloy composition, thin film analysis and FIB cross sectioning. Lab scale plating is possible in our in house plating tools allowing for standards development, feasibility studies, and demonstration of the MacDermid Enthone MICROFAB processes. Our Innovations Lab in Taiwan provides 300mm full wafer plating and reflow capabilities for customer demos.

MICROFAB WLP Processes

MacDermid Enthone MICROFAB WLP processes meet 3D packaging requirements and enable greater device reliability. Specifically formulated to meet WLP cost, size and performance challenges, MICROFAB processes include copper, tin, nickel and gold electroplating chemistries for copper bump/copper pillar/post, copper redistribution layers (RDL), and through-silicon via (TSV) fill. Each technology supports a broad spectrum of package applications that ranges from MEMS, RF filters and PAs to leading edge FOWLPs, high die count memory stacks and high performance RF modules.

MICROFAB chemical technologies are manufactured at world class, ISO-certified facilities strategically located throughout the globe. Each process is formulated, packaged, and quality controlled per stringent semiconductor industry requirements.
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Wafer Bump / Pillar Stack (Cu, Ni, SnAg, Au)

- Copper processes engineered for high-speed pillar and copper stud/UBM applications
- Wide current density range to meet throughput requirements
- Optimized to meet customer specific performance criteria (e.g. WID, WIF, WIW, deposition rate)
- Supports broad range of feature diameters and heights
- Hybrid / versatile chemistry capable of flat, domed or dished morphology

Copper RDL & “2-in-1” RDL

- Delivers uniform metal distribution for the most sophisticated wafer layouts.
- Maintains deposits with low internal stress with wide additive operating window
- High deposition rate with thickness uniformity
- Hybrid chemistry to support multiple planar features such as “2-in-1” and “3-in-1”

Through-silicon Via

- Meets the decreased size/miniatrurization, high performance requirements for advanced and emerging 3D – IC technologies.
- Provides enhanced electrical and thermal conductivity
- Delivers robust defect-free fill performance with low cost-of-ownership

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