

Single Step Metallization Process for the Filling of Through Holes with Copper

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ABSTRACT

This paper will discuss a copper plating process capable of filling through holes with solid copper in a single step. This technology can be utilized for applications such as core layer through hole filling with minimal surface copper build up for HDI technologies and thermal management of heat sensitive electronics. The advantages of the single step filling process benefit both the technology and the fabricator. The ability to fill core layer copper through holes of a variety of aspect ratios without voids and with minimal surface copper plating enables improved fine line resolution for HDI and IC substrates. For thermal management of closely packed heat generating sources, the presence of a solid copper structure offers greatly enhanced thermal conductance versus conventional technologies in drawing heat from operating devices and dissipating it throughout the printed circuit board. From a processing standpoint, the single step copper filling technology is capable of filling various through holes in a fraction of the time compared to conventional DC copper plating technologies, greatly increasing potential throughput. In certain applications, the copper filling technology can eliminate complete processes, greatly simplifying the manufacturing process.

This paper will discuss in detail, the various aspects of the single step copper filling chemistry and the advantages this technology can provide versus conventional systems. Presented will be the current capabilities and limitations of the process as well as design guidelines.

Key words: Bridge, Pulse Plating, Copper Electroplating, Thermal Management, Core Layer, Copper Through Hole Fill

INTRODUCTION

As designers continue to increase the functionality of electronic devices, printed circuit board substrate fabricators have been forced to develop new fabrication techniques to accommodate the miniaturization and densification of circuitry and the unique requirements that come along with it. This has resulted in the need for new design features utilized in the printed circuit board. Extremely fine lines and spaces with critical trace profiles and coplanarity for controlled signal impedance, filled blind microvias and through holes for vertical signal routing to maintain short

signal distances for maximized clock speeds, and thermal vias for the management of the heat concerns associated with more tightly packed electrical components are examples such features. These new design features have required the development of novel metallization chemistries capable of meeting the stringent needs of these new substrate architectures in terms of capability, versatility, and reliability.

Through holes have long been a means of electrical interconnection between layers of a printed circuit board, both as a stand-alone feature and as a base upon which to build further layers (i.e. buried via). As a stand-alone feature, the through hole is plated with a copper deposit thick enough to provide the necessary strength and electrical performance to survive the rigors of assembly and usage. In designs where further build up layers are required, it becomes necessary fill the through hole with material for structural integrity. The current options of filling through holes for core layer build-up are plugging, DC plating, or two-step copper through hole filling. The single step through hole fill process described in this paper is an improvement over these alternatives and can be used to simplify the current manufacturing process of some PCBs.

Plugging

To plug a hole, the through holes are first plated with copper for electrical performance. Then the filling is accomplished in a separate process by forcing a conductive or non-conductive resin, typically epoxy based, into the plated through hole followed by curing and planarization of the epoxy plug. This plug is then plated over with electroless copper before further build up.

With the advent of HDI (High Density Interconnects) and the continued evolution towards circuit miniaturization and densification, drawbacks to resin filling of through holes have become evident. As through holes decrease in size, it becomes much more difficult to get the resin into the through holes to fill them completely, resulting in a weakened structure on which to build further layers. In addition, finer line circuitry with smaller features requires much tighter dimensional tolerances for proper registration, making mechanical planarization of the plugged through holes much less desirable.

From a reliability standpoint, the coefficient of thermal expansion mismatch between the resin plug and surrounding copper and the smaller contact areas for metallic bonding between layers in these smaller features can result in higher rates of mechanical failure during thermal excursions. In terms of thermal management, the plugging material offers very limited thermal conductivity versus a solid, metal filled through hole as shown in Figure 1.

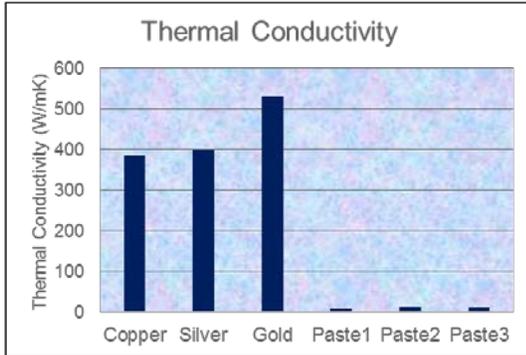


Figure 1: Comparison of thermal conductivity

DC Plating

A second option currently used is direct current (DC) plating. This process allows simple through holes to be filled entirely with copper and removes the need for pastes. The process is typically used in X-shaped, laser drilled through holes. In the direct current plating of laser drilled X-vias, core layers are laser drilled from each side resulting in holes with a tapered middle. The tapered hole wall allows the copper deposit to thicken in the middle of the hole to the point where the two sides of the hole wall meet and grow together, subsequently filling the remainder of the hole.

This style of plating has very limited capability and cannot plate straight mechanically drilled through holes. Factors that limit using this style of plating include panel thickness (typically less than 0.2mm), and the number of holes on the panel. DC plating also has much higher plated copper, often results in an uneven surface profile, and has increased chance of creating a seam cavity (voiding).

Two-Step Through Hole Filling

The third option is a two-step through hole filling process. This two-step process starts by creating a bridge of copper that closes the through hole, creating essentially two blind vias, and then going into a second bath fill these vias. These solutions contain typical components such as copper sulfate, sulfuric acid, chloride ions, and additives. The bridge bath is designed with high copper concentration and low acid. The addition of a brightener for acceleration, and a wetter for suppression, help the pulse bath create the initial bridge. The second copper bath, designed for the filling of the vias also includes a leveler, for flat plating and improved via filling. Pulse rectification is used in the first plating bath to disrupt the equilibrium formation of the additive films and redistribute current into low charge density areas. These pulse

waves consist of a cathodic, or forward, cycle, followed by a series of short, high current density anodic, or reverse, cycles. The bridge cycles used are based off this concept. Over time, these repeated waves plate a thick area of copper in the center of the hole with minimal copper plating on the surface. Eventually these two thick portions meet and create a bridge, as seen in Figure 2. The panel is then switched to the second bath and plated in DC mode, which fills the remainder of the hole. This creates a solid through hole filled with copper.

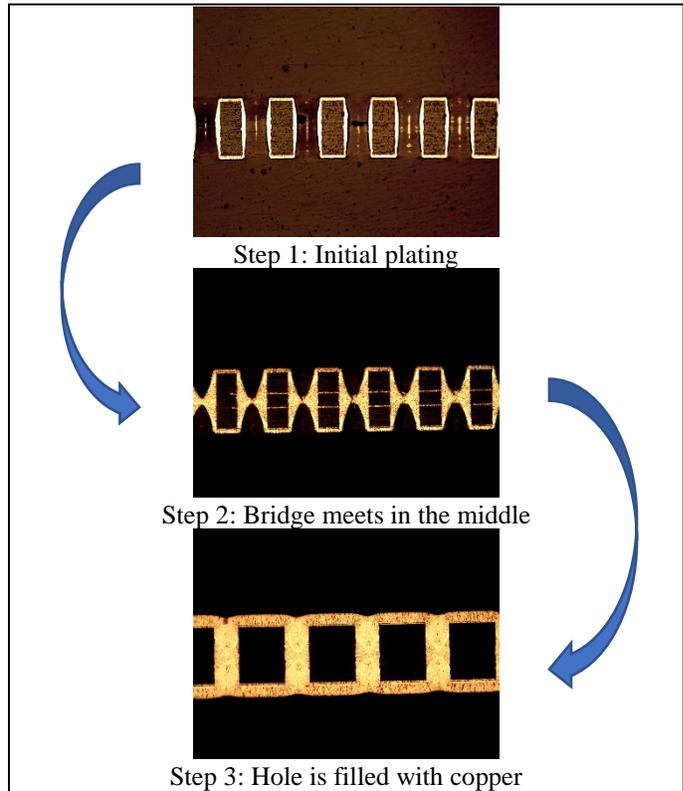


Figure 2: Through Hole Filling Plating Progression

ONE-STEP THROUGH HOLE FILLING

The one-step copper through hole filling process is a novel process created where the pulse and DC baths have been combined into one bath. Using a novel leveler, a pulse plating bath is made into a new plating solution that can still bridge through holes and has the capability to fill vias. This single step process still uses the pulse cycles, but then directly converts to DC without removing the panel. By using a one-step process, there is no separate processing between the initial bridge formation and the filling of the created vias. This reduces the chance for oxidation or contamination at the interface between the pulse cycling and DC plating.

Larger vias take more copper to fill, and there are limits to the copper filling of through holes utilizing electrolytic plating including the single step process. Due to this, it is important to adjust the pulse cycles to limit via size as much as possible. The leveler is designed to withstand the aggressive pulse cycles and its damaging effect on organics. Modifications to the pulse cycle can help alter the shape of the resultant via as well as to make the via easier to fill. With

less copper on the surface and a flatter profile, the panel can avoid unnecessary etching and planarization steps.

In Figure 3 below, a series of SEM photographs of the grain structure within the filled copper feature is shown. Unlike two-step processes, there is no interface observed between the bridging and filling stages of the process. Photos were taken at higher magnification at the knee of the hole, the center where the deposit bridge met, and at the point where the plating cycle switched from pulse to DC. At no point in these photos is an interface visible which could lead to a separation problem.

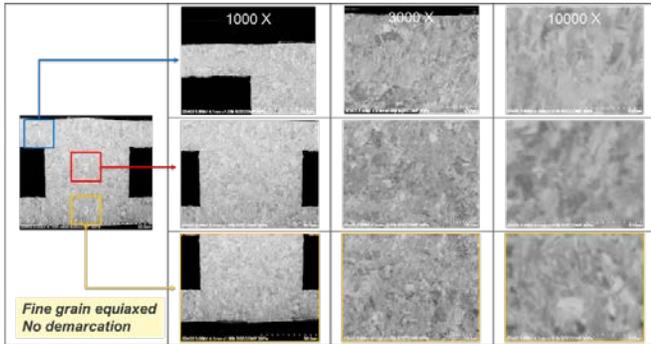


Figure 3: SEM of Single Step THF

Core Layer Requirements

The typical requirements for through hole filling are complete cavity free fill and a flat profile on the surface. The filled copper through hole creates a very strong, stable structure upon which to build further layers. The solid copper resulting from through hole filling has little to no tendency to crack under thermal stressing and the low coefficient of thermal expansion of the copper versus epoxy plugging material reduces the overall stress on the structure. All interfaces are also metal to metal bonds, representing the strongest possible layer to layer bonding strength. Additionally, minimization of surface copper plating is required for HDI capability and helps eliminate the need for subsequent copper reduction and planarization steps.

Thermal Requirements

Thermal management has become more critical as circuit board design has gotten smaller and the boards deal with increased heat due to higher densities of components. A complete copper hole is ideal for the largest heat sink in a small area.

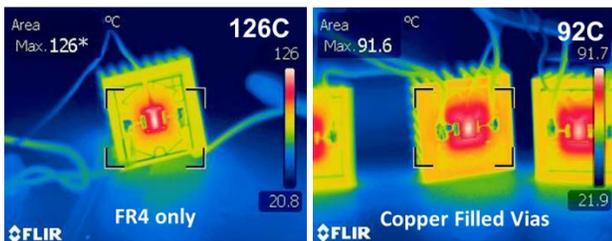


Figure 4: FR4 only vs Copper filled vias

In Figure 4, there is an example of an application of copper filled through holes for thermal management in LED applications. The temperature of the FR4 material only is significantly hotter, at 126°C, and more focused in the center of the component. With copper filled holes the temperature is limited to 92°C and is more spread out through the component. The improved thermal management allows for higher device efficiency, truer color, and longer device life.

Equipment Requirements

A limiting factor in two-step copper through hole filling processes is the special tank design. This design is expensive and limited to a few panels at a time. The single step through hole filling process can use either this tank design or a modified VCP line. As a result, the single step process allows for a reduction of equipment that requires up to 40% less floor space than the two-step equipment. This also reduces maintenance time and up-front cost of new equipment.

PANEL DESIGN

Factors

The current process is focused on laser drilled X-holes and mechanically drilled through holes. The process has been optimized for panels thinner than 0.4mm but can go as thick as 0.6mm. Panel design has a significant effect on which cycles work best so cycles need to be adjusted for each new design. There are several factors that influence the ability to fill through holes that a designer should be aware of when laying out a panel. Among these are hole diameter, panel thickness, aspect ratio, pitch, and density of holes.

Hole Diameter

The hole diameter is critical to the ability to close the center of the hole for cavity-free filling. If the diameter of the hole is too narrow, the initial portion of the cycle will tend to form multiple bridges resulting in a double cavity effect. Typically, this will become prevalent in hole diameters of less than 0.15mm, as shown in Figure 5.

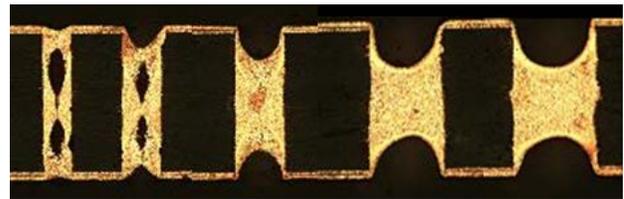


Figure 5: Double Cavity

Though the process can bridge a substantial distance, a realistic limit to hole diameter is approximately 0.45mm. Above this, the size of the blind microvias formed are too large to adequately fill without exorbitant amounts of surface copper as illustrated in Figure 6.

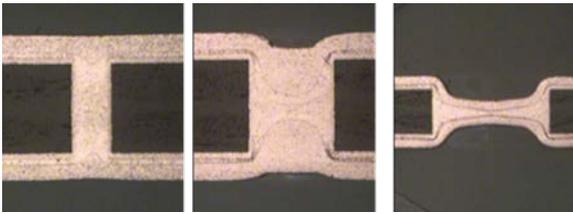


Figure 6: Increasing Hole diameter

Panel Thickness

Thicker panels create a host of issues due to the limitations of the plating baths. As panels get thicker, the total copper plating required to completely fill the hole increases exponentially. As panel thickness increases, one needs to consider the volume of the through hole cylinder that needs filling. One must also consider the size of the blind microvia formed after bridging and its ability to be filled with a minimal dimple. This will require additional surface copper and plating time. As the panel thicknesses approach 0.5mm or more with hole diameters from approximately 0.15 – 0.35mm, plated surface copper to fill the through hole can be greater than 100µm. This will require additional plating time. See Figure 7.

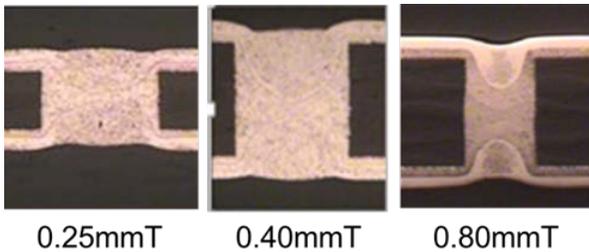


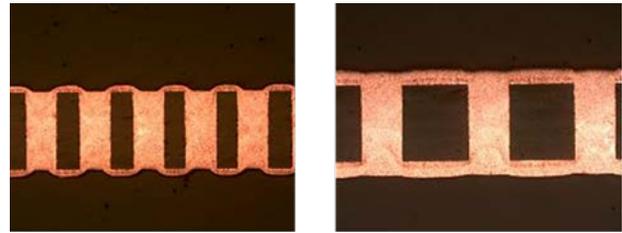
Figure 7: Panel Thickness

Aspect Ratio

The aspect ratio of the hole, in conjunction with the hole diameter and panel thickness, play a large role in the through hole filling process. As aspect ratios increase at lower hole diameters, the pulse portion of the cycle will tend to form multiple bridges resulting in cavity formation, see Figure 5. A general rule with aspect ratios is to target less than 4:1.

Pitch

The pitch causes a similar phenomenon where holes closer together must be plated for longer to create a solid copper structure and complete fill. The larger the block of holes with a tight pitch, the lower the net current density reaching the center of the holes will be. This can cause issues with overplating on the outside of the block of through holes with minimal filling in the center of the block. Reducing current density can help minimize this effect but panel design may need to be modified. The difference in plating between pitch dense vs isolated holes is shown in Figure 8.



Dense Isolated

Figure 8: Pitch- dense vs isolated holes

Hole Density

The total number of holes on a panel can have a large effect on the capability to create a solid copper block. With increasing numbers of holes, the chances of cavities in holes increases as does the difficulty in achieving a complete fill. When looking at blocks of holes, the center of the block will experience lower current density compared to the outer ring. This can create issues of overplating on the outside edge without complete fill on the inside of the block. This creates a situation where the outside edges of the block will be overplated and have a high chance of having cavities while the center of the block will not have complete fill. High versus low hole density areas are shown in Figure 9.

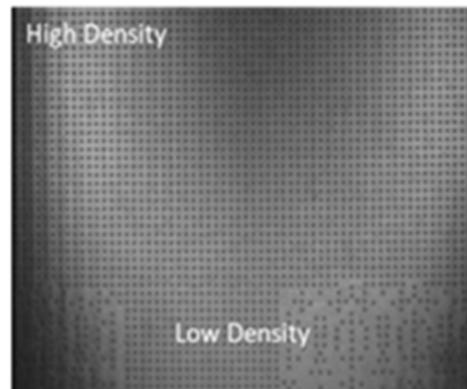


Figure 9: High vs Low Density areas

RESULTS

A large amount of testing has been completed on various boards to evaluate process performance over the variety of factors mentioned above. In this section, we highlighted a few examples of successful complete filling to show the current capabilities. Testing is continuing to expand the available portfolio, but the process is very specific to panel design. For this reason, minor modifications may need to be made to the plating cycle, current density, and bath conditions to expand capabilities.

Single Step Through Hole Fill Capabilities

Shown in Figure 10 is a laser drilled x-hole with a 70µm opening and 100µm thickness. This panel design was plated with a conventional DC process and with the single step process. It took 50 minutes to complete the fill with the DC process and only 38 minutes to complete the fill with the single step process. Additionally, the final profile is flatter

with the single step process over the DC with less copper plated on the surface.

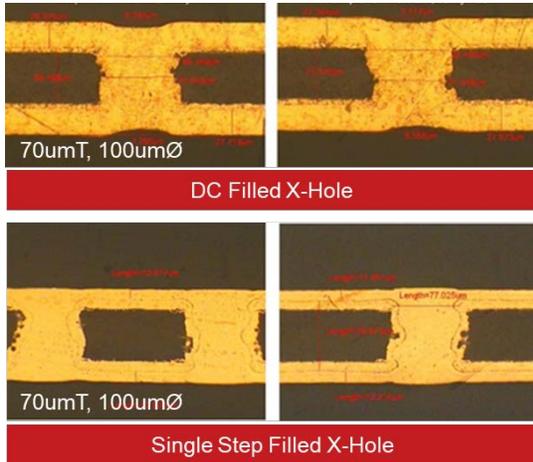


Figure 10: DC vs Single Step Laser drilled

As previously mentioned, mechanically drilled through holes are typically more difficult to fill due to the straight hole walls compared to the x-shaped design which has a reduced neck in the hole and can influence reliability. In Figure 11, the top left shows an example of a laser drilled hole vs the top right with a mechanically drilled hole. The two lower photos show a mechanically drilled hole that has no dimple and 25µm of surface copper.

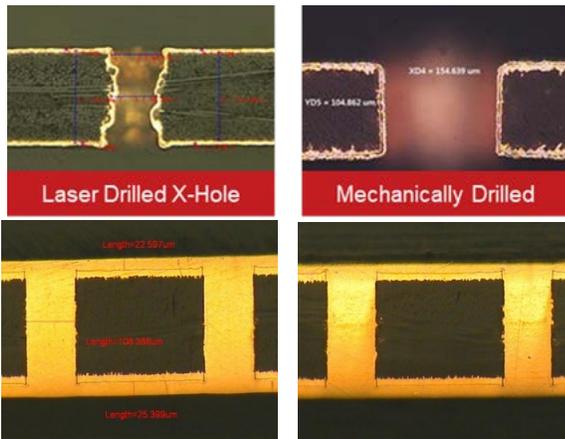


Figure 11: Example of Laser vs Mechanically drilled

On the high end of the process capability, Figure 12 shows an example of a thicker mechanically drilled test board. The board was 0.5mm thick with 0.25mm diameter holes and had very dense hole population. Due to the difficulty of this board, the surface copper is much thicker, around 150µm, and plated for 9 hours. The panel was filled completely without dimples.

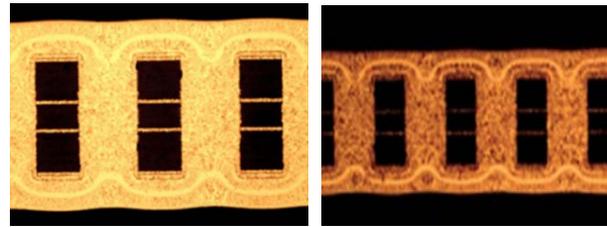


Figure 12: Example of a high density 250x500µm hole

Single Step- Viafill

For increased versatility the single step process can also be used for viafill. The viafill performance for the through hole plating bath is good on vias up to 5x4mil. In the below Figures 13 and 14, a set of vias were filled with 15µm of plated copper, with minimal dimple.

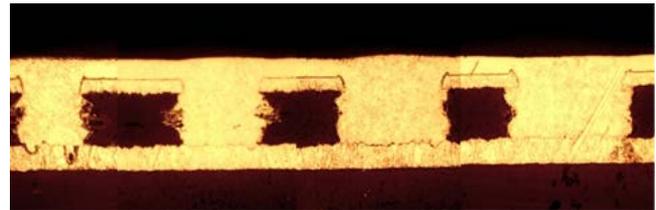


Figure 13: Varying microvias 3x3mil to 6x3mil

Plating thickness	φ 100um x D 80um	φ 125um x D 100um
15 um		
20 um		
Dimple < 5um		

Figure 14: Varying via sizes with 15µm and 20µm of plated copper.

Blind microvias, with dimensions of 5x4mils and less fill very well with less than 15µm of surface copper. By increasing the plated copper to 20µm, the dimple is reduced to less than 5µm.

DISCUSSION

Single step copper through hole filling has many advantages over DC plating and the two-step copper through hole filling processes. DC plating is often too limited and time consuming to be used in real-world applications. High lead-times and minimal production throughput make mass production impossible, and the process does not create the flat profile required for build-up. Voiding also becomes a major concern and panels need to be monitored closely to verify voiding is not occurring. The two-step process improves on this by expanding the capability significantly

and reducing plating time. But the two-step process is limited due to specific equipment that is needed which has a large footprint in a board shop while also introducing multiple copper grain interfaces.

The single step process solves these problems. It has an increased capability over standard DC plating as it has shorter plating times and uses less copper. The plating speed is up to 140% faster than using a DC process on thin core boards. The filled holes also have a flat profile which makes it easier to further build on. It also removes the need for specialized equipment and can be run in a standard VCP, vertical continuous plating line, with minor modifications. Lastly, there is no need to transfer the panels during plating to a separate viafill tank, further reducing both footprint and time and creating a solid copper structure without grain boundaries due to multiple plating steps.

Filling Capabilities

Hole Diameter (mm)	Panel Thickness (mm)															
	0.06	0.07	0.08	0.10	0.15	0.20	0.25	0.30	0.40	0.50	0.60	0.80	1.00	1.20	1.40	1.60
0.10	X	X	X	X	X	X	X	X	X							
0.15	X	X	X	X	X	X	X	X	X	X	X					
0.20	X	X	X	X	X	X	X	X	X	X	X					
0.25						X	X	X	X	X	X					
0.30						X	X	X	X	X	X					
0.35						X	X	X	X	X	X	X				
0.40						X	X	X	X							
0.45						X										
0.50																
Surface Copper (um)	10	10	10	15	20	20	25	30	35	100	150	160				

Figure 15: Capability Chart

The filling capability of the through hole fill process ranges from panels as thin as 0.06mm to panels as thick as 0.80mm as shown in Figure 15. On the thinnest panels, plating can be done with aspect ratios of less than 1:1 up to 3.3:1, while on the thickest panel a more limited range is possible. The surface copper on thin panels is minimal, around 10-20µm. Focus in the market has been on the 0.10mm to 0.30mm thick. Plating times for this range are around thirty to seventy-five minutes.

Panels that are 0.20, 0.25, and 0.30mm have been tested more thoroughly and a wider range of aspect ratios is available. For the 0.20mm thick panel, aspect ratios can range from 0.5:1 up to 2.25:1. As the hole diameter gets wider it becomes slower to create the initial copper pinch point requiring more surface copper.

As panels get thicker (>0.5mm), the amount of surface copper required goes up significantly, up to 160µm at the thickest. With the thicker applied copper, the plating time also goes up substantially. Plating times for these thicker panels can go up to 6 hours. The minimal dimple depth that can be created also increases with thicker panels due to the bath's capability.

With thicker panels the resultant vias are harder to fill, typically deeper vias than normal, and this creates a larger dimple.

Testing is ongoing to expand the available panel ranges with alternate cycles and current densities. Currently the testing has all been done on panel plate, but alternate formulations are being worked on for pattern plate. Engineers must consider the factors that influence the through hole fill process when designing circuit boards for the process to work correctly. Things to consider are the factors noted above. As board design gets smaller and more complicated these factors must be considered more to make sure the plating is possible in a reasonable amount of time.

RELIABILITY

Complete copper filling is critical for build-up of core layers and therefore must be able to handle a significant amount of stress. A major factor effecting reliability is voids or cavities.

The process was evaluated with cross sections and X-ray analysis to determine performance. Panels plated using this process underwent standard IPC testing to verify it could handle the stress of reflow and assembly.

X-Ray Inspection

X-ray analysis allows an entire panel to be evaluated for large cavities rather than using multiple microsections. In Figure 16, X-ray inspection is used to show complete filling of through holes when board designs were within the process capabilities.

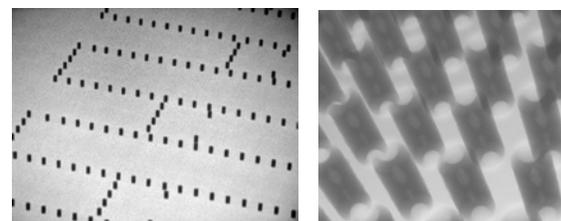


Figure 16: X-ray of cavity free plating and X-ray of plate with cavities

IPC Standard Testing

Testing of the through hole fill bath showed good reliability. Six times solder shock at 288°C for 10 second per IPC

specifications showed no cracks. Five times IR reflow testing also showed no cracks. The tensile strength was 45-48K psi, and the elongation percent was 18-23%.

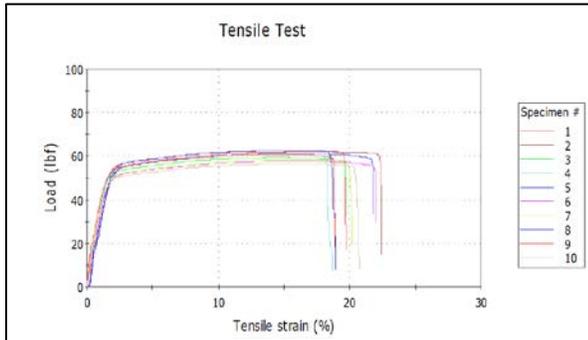


Figure 17: Tensile and Elongation Results

CONCLUSION

There are significant advantages of the single step copper through hole filling process that benefit the fabricator in the designing of circuit boards. The plating performance this process is excellent and has no interface from the pulse to dc plating crossover. This eliminates the risk of introducing a new failure point and reduces the chance of voiding. In thin boards, the surface copper can be minimized to reduce or remove plating steps. The finished holes have little to no dimple, allowing for subsequent layers to be stacked with ease. The process can also be used to fill blind microvias as a standalone process.

The single step process simplifies the plating process by reducing the number of plating tanks and simplifies the overall fabrication process by eliminating or reducing subsequent planarization and copper reduction steps.

It is important that the design engineer understand factors that affect the filling process such as the shape of the through holes, diameter, aspect ratio, pitch and hole density in order to design a board utilizing the technology for ease of fabrication.

The single step through hole filling process offers a novel and easier way for circuit board manufacturers to create solid copper structures in new sizes, shapes and areas. This will enable new board designs for next generation thermal technology along with improving core layer structural integrity.

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