

PIT RESISTANT ACID COPPER ELECTROPLATING PROCESS FOR FLASH ETCHING

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ABSTRACT

Rapidly changing products and applications for electronics continually push the requirements for IC substrates and PCBs. To meet these requirements industry leaders are using technologies such as High-Density Interconnects (HDI), Semi-Additive Processing (SAP), and modified Semi-Additive Processing (mSAP) to meet the requirements of tomorrow. These technologies help maximize the PCB real estate usage by allowing fabricators and designers to perform multilayer buildup with increased circuit densities. During this process, multiple metallization and etching steps are required to achieve desired designs.

As the number of layers in the circuit board increases, so does the chance for critical defects to occur. Hence, a great deal of attention has been paid to the Cu deposit and how it reacts to subsequent etching processes. Higher density interconnect technologies may require many etching steps. During chemical etching, variations in etching rate across the surface of the copper can result in pits forming. This phenomenon is known as V-pitting. These defects can cause severe reliability issues in the final product. Fabricators are currently trying to resolve these issues by baking the plated panels for several hours to alter the crystal structure of the copper through annealing, but this increases the process cost and negatively affects production output. Therefore, innovative Cu electroplating solutions are required to produce Cu deposits that etch consistently. The purpose of this study was to investigate the underlying mechanism of V-pitting and to develop an electroplating process that reduces pit formation while also being robust enough to perform consistently in large scale production.

KEYWORDS: Flash Etching, V-pitting, Reliability, Via Fill, Trough hole, Pattern Plating, metallization

INTRODUCTION

Copper electroplating is broadly used within the electronics industry to create elaborate structures and connectivity that meets the needs of complex circuit designs. Various processing techniques, such as SAP and mSAP are utilized by fabricators to create multilayer buildup designs like those shown in Figure 1. During these processes, multiple

metallization and etching steps are required. In this way, the etching steps have become essential to creating uniform surfaces with strict control over surface Cu thickness.

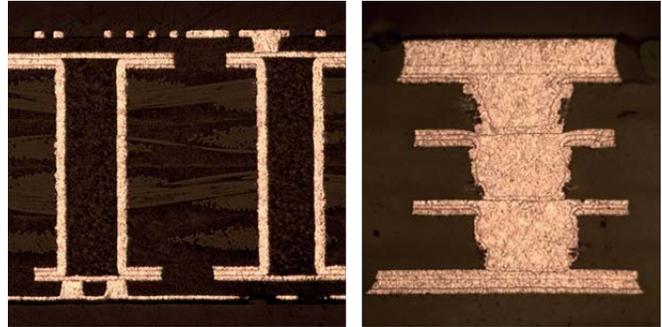


Figure 1. Multilayer buildup. Several processing layers are visible in the cross-section.

During multilayer buildup, it is essential to create defect free deposits. Although an initial deposited Cu surface may appear defect free, the subsequent etching steps in the manufacturing process may result in pinholes or pits forming. Depending on design, multilayer buildup boards may go through many etching steps. During which, uneven etching, pinhole formation, pitting, and V-pitting, become significant issues. These defects can cause severe reliability issues in the final product, such as poor stacking over pits or pinholes, reduction in fine line cross-sectional area resulting in poor signal propagation, and creation of stress points that lead to potential cracking. Figure 2 shows the pits that are typically observed after etching on conventional electrolytically deposited Cu. This phenomenon is called “V-pitting” due to the characteristic V shape of the pit. When observed from above, typical pits on the surface appear circular. When they are cross-sectioned, the characteristic “V” shape can be seen. In this study, we focused on the formation and prevention of V-pits, although other pit geometries were also observed.

Many manufacturers observe these pits and have tried to mitigate them by annealing boards between plating and etching. However, this is time and energy intensive, so creating an electrolytic system that reduces pits is highly desirable.

The mechanism by which voids form was investigated by Ho et al. They showed that the formation of these pits is correlated to contaminants in the Cu deposit. The contaminants cause channels or voids, which allow pits to form during etching (1) (2). The results we observed agree with this mechanism. When intentionally applying contaminants to areas on the Cu clad surface prior to electrolytic plating, high volumes of V-pits were observed in these areas after plating and etching. Functional additives in the electroplating bath not only control the morphology, but also affect the rate at which organic impurities are incorporated into the deposited Cu. These additives include CuSO_4 , Cl^- , H_2SO_4 , wetters, levelers, and brighteners (3). In this study, we show that by controlling the functional additives we can greatly reduce the amount of V-pits formed during flash etching processes while matching the performance of incumbent via filling/through hole plating systems.

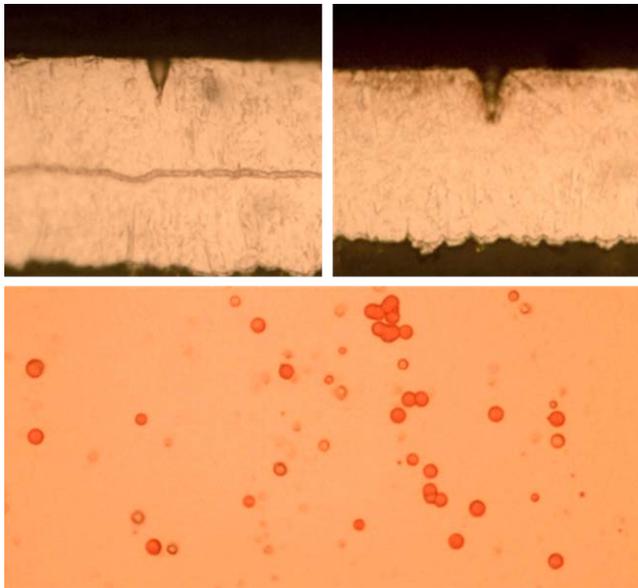


Figure 2. Surface with typical pitting image from above and a cross-section of pits showing the characteristic “V” shape

METHODS

Performance of additive systems was determined by plating test panels and following reproducible etching procedures. Plating runs were carried out in 8L cell and 200L pilot tank, utilizing insoluble anodes. Baths were made up, dummy plated for 1 Ah/L, and adjusted to specifications before plating panels. Each panel went through a standard cleaning procedure, shown in Figure 3.



Figure 3: Pre plating cleaning procedure

Acid Copper Plating

The optimum operating conditions for balanced V-pit resistance, via fill, and through hole plating performance

were determined by performing a DOE. Table 1 shows operating ranges and optimum levels that exceeded the performance of conventional via fill/through hole systems.

Table 1: Bath components, addition levels, and plating conditions

Parameter	Range	Optimum
Anode Current Density	1.0 – 3.5 ASD (10-32 ASF)	2.2 ASD (20 ASF)
Duration	Variable to target surface Cu	50 minutes
Temperature	20 - 27°C (68 - 80°F)	23°C (73°F)
Wetter	9 - 25 mL/L	10 mL/L
Brightener	0.25 - 1.0 mL/L	0.5 mL/L
Leveler	15 - 35 mL/L	25 mL/L
Copper Sulfate ($\text{CuSO}_4 \cdot 5 \text{H}_2\text{O}$)	230 - 250 g/L	250 g/L
Free Sulfuric Acid Electronic Grade	45 - 65 g/L	50g/L
Chloride Ion (Cl^-)	40 – 60 ppm	50 ppm

Flash Etching Procedure

A peroxide-based etching solution was used to etch the Cu to the desired thickness. The etching solution was comprised of 10% peroxide (50% solution), 15% sulfuric acid, and 4% stabilizer. During etching, the solution was maintained at a temperature of $30(\pm 2)$ °C. After plating was complete, panels were rinsed with DI water and dried with compressed air. Panels were allowed to sit for exactly 15 minutes at room temperature (21-24°C). Flash etching was then carried out on the fresh deposit. The etching rate for this solution was ~ $3\mu\text{m}/30 \text{ sec}$. Separate samples from the panel were placed in the etching solution for 30 and 60 seconds, respectively, in order to etch 3 and 6 μm of the surface Cu. Finally, the pieces were dried with air and analyzed immediately under a microscope.

Cross Section Analysis

Cross-section samples were cut from the board using a punch and pre-ground to reach the specific structures on the board. The samples were stabilized using plastic sample holders and the boards were aligned perpendicular to the grinding surface. A fast-cure acrylic resin was used to mount the samples. A ratio of 1-to-1, hardener-to-resin, was used to provide optimum penetration and a quick cure rate (10-15 minutes). After the sections hardened, they were subjected to grinding, polishing, and microscopic inspection.

Test Panels

Test panels from different manufacturers, and with different via sizes, were used during the evaluation. The panel thickness was 0.8mm and via diameters ranged from 75 – 175 μm . The via depths were either 75 or 100 μm . All geometries for each test board thickness were plated at the same time and in the same tank. The dimple is defined as the difference in height between the surface Cu and the center of the via. An example of this measurement can be seen in Figure 4. A via with Cu protruding above the plane of the surface Cu is defined as having a bump.

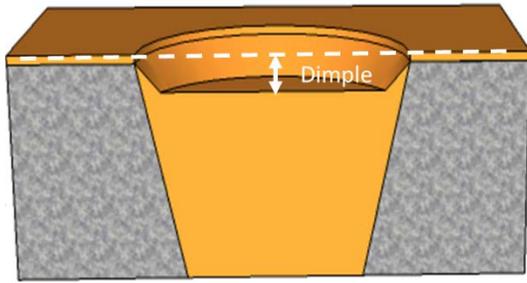


Figure 4: Via geometry and dimple measurement.

Through hole performance was evaluated by measuring the microdistribution % and knee %. The microdistribution is defined as the ratio of the average copper deposit thickness in the center of the through-hole to the average copper deposit thickness at the surface. It is calculated according to Equation 1.

Equation 1. Microdistribution calculation.

$$\frac{(C + D)/2}{(A + B + E + F)/4} \times 100\%$$

The knee % is defined as the ratio of the thickness at the knee and the thickness on the surface and is calculated using Equation 2. Figure 5 shows the specific location of all measurement points for both microdistribution and knee %.

Typical via fill baths can have knee % values below 50%. However, the formulation tested yielded knee % greater than 80% for 4:1 aspect ratio through holes while filling a 120x100 μm via with a dimple of less than 5 μm.

Equation 2. Knee % calculation.

$$\frac{\left(\frac{C1}{A}\right) + \left(\frac{C2}{B}\right) + \left(\frac{C3}{E}\right) + \left(\frac{C4}{F}\right)}{4} \times 100\%$$

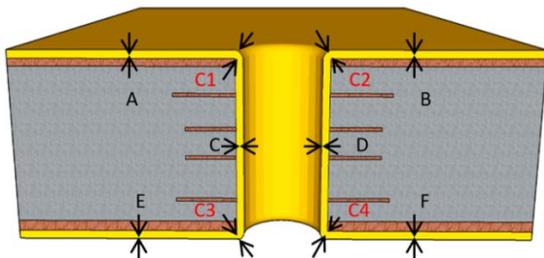


Figure 5. Microdistribution % and knee % measurement locations

Physical & Thermal Properties

It is critical that the deposited Cu is physically robust enough to withstand the physical demands of PCB applications. To evaluate this, the two primary physical attributes evaluated are tensile strength and elongation %. These properties correlate to the deposit's thermal stress tolerance. The

organic additives (suppressor, grain refiner, and leveler) will affect these characteristic physical properties.

Equation 3. Mean average cross-sectional area (in²).

$$\frac{\text{Weight of the sample (lbs)}}{\text{Length of tensile sample (in)} \times \text{density of copper (g/in}^3)}$$

Equation 4. Tensile strength calculation.

$$\frac{\text{Maximum load (lbs)}}{\text{Mean cross sectional area (in}^2)}$$

Equation 5. Elongation percent calculation.

$$\frac{\text{Length at break} - \text{Original gage length}}{\text{Original gage length}} \times 100\%$$

Tensile strength and elongation were measured according to the IPC TM-650, 2.4.18.1 standard. A stainless-steel panel was plated with the current formulation. Sample strips were then removed from the plated panel and baked in an oven at 125 °C for four to six hours. An Instron pull tester instrument was used to test the strips. The measurements were used to calculate tensile strength and elongation % using Equations 3, 4, and 5.

SEM/EDS Analysis

SEM/EDS analysis was performed using an Ultra dry Hitachi S-3400 VP / ESED-Environmental Secondary detector. When EDS was performed, a working distance of 10mm was used, and scans were performed at 5KX. Data was evaluated with Noran Pathfinder software. Samples were prepared by mounting on a platform with carbon and copper tape to ensure conductivity to the mount.

RESULTS & DISCUSSION

V-pitting Performance

Conventionally deposited Cu develops V-pits broadly across the surface after etching. The pits are both dispersed and concentrated in macroscale agglomerations. These V-pits occur on a such a large scale that it is not possible to quantify them. The etched surface of the conventional Cu can be seen in Figure 6.

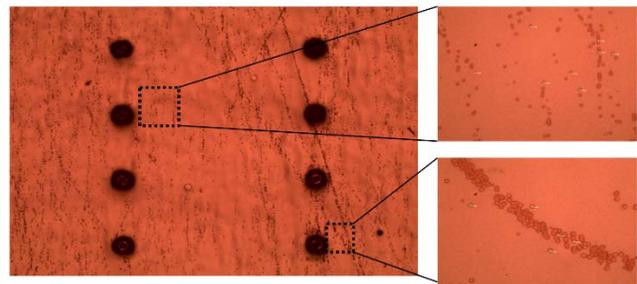


Figure 6. Conventional Cu electroplated deposits after 3 μm flash etching. Isolated and bundled v-pits were observed.

The novel formulation creates a surface that is very pit resistant. The number of pits on the surface is drastically reduced. Even without a method to quantify the V-pit frequency, the improvement is apparent. Figure 7 shows the surface of the novel formulation after being etched.

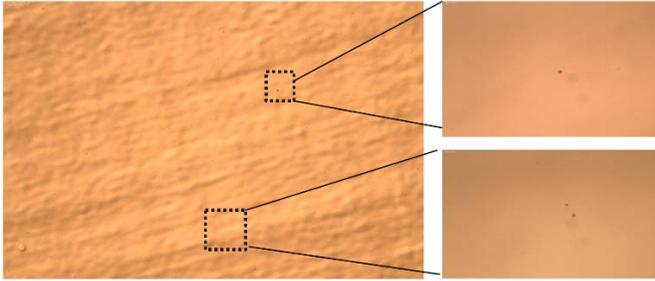


Figure 7. Cu deposit after 3 μm flash etching, electroplated with the new formulation. Hardly any v-pits were observed.

During our plating experiments, we observed that surface contamination on the board, prior to cleaning, can lead to surface defects in the electrolytically deposited Cu. These areas were more likely to have high concentrations of V-pits. Our team intentionally applied fingerprints to the surface of boards to illustrate this. The novel formulation was less likely to have surface defects in these areas compared to the conventional formulation. Figure 8 shows areas on panels where fingerprints were applied to the surface of panels, prior to cleaning. The boards were then cleaned and plated. Surface defects can clearly be seen on the board plated with the conventional formulation, whereas the novel formulation creates a uniform deposit without defects.

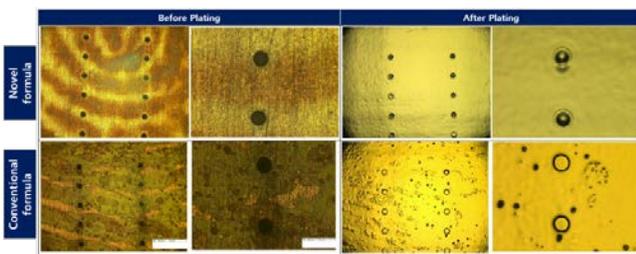


Figure 8: Panel surface where fingerprint was applied before and after plating

The surface defects are also more prone to forming V-pits after etching. The areas that had fingerprints applied in Figure 8 were then etched down by 3, 6, 9, and 12 μm . The surfaces were then imaged and shown in Figure 9. The novel formulation etches very evenly, and no v-pits develop. The conventional formula develops v-pits after 3 μm and these V-pits grow in size as etching continues.

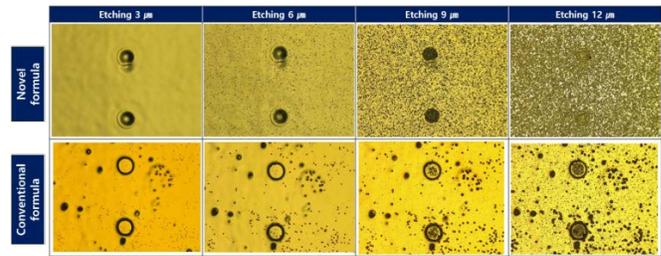


Figure 9: Fingerprint areas after surface etching

Multiple types of test panels were utilized during our evaluations. Certain test panels had pits that formed specifically on filled microvias. We discovered that the identity of the boards and how they were processed influenced the preferential pitting of filled vias. Furthermore, the via diameter was correlated to the preferential pitting. Smaller vias were more likely to have pits than larger vias. Figure 10 shows examples of the preferential pitting of filled vias. The geometry of these preferential pits was not the typical “V” shape observed on the general surface and they were much deeper than usual.



Figure 10: Preferential pitting on filled vias

Using SEM/EDS, the unplated boards were inspected for signs of contamination. Figure 11 shows the presence of contaminants including Br, Ca, C, O, and Si. The Si and O could be explained by glass bundles protruding from the side of the via, even though the entire inside of the via should be covered with continuous Cu deposited by an electroless process. The presence of Br, Ca, and C are likely due to incomplete cleaning during board processing. We evaluated boards before and after our standard pre-plating cleaning procedure, and the contaminants were still present after cleaning.

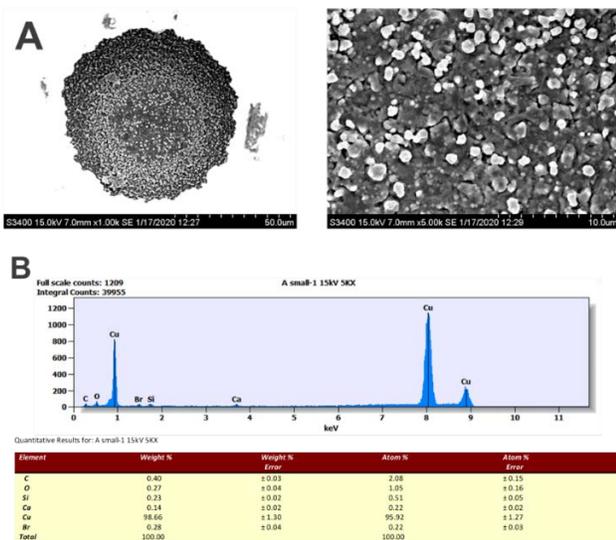


Figure 11: A) SEM micrograph of a via from above showing the non-uniform bottom. B) EDS spectrum of the bottom of a via showing the presence of multiple contaminants.

Via Fill & Through Hole Performance

The novel formulation needed to adequately plate certain features based on specific applications. The application requires that vias with certain dimensions (100µm x 75µm, 100µm x 100µm, and 125µm x 100µm) must be filled with a dimple that is less than 10µm. The formulation also needed to plate 200µm x 800µm through holes with microdistribution and knee % greater than 80%.

Optimum operating conditions were determined by conducting a DOE. At the optimum conditions, the plating performance exceeded the via filling and through hole plating requirements. An example of typical and reproducible performance is shown in Figure 12.

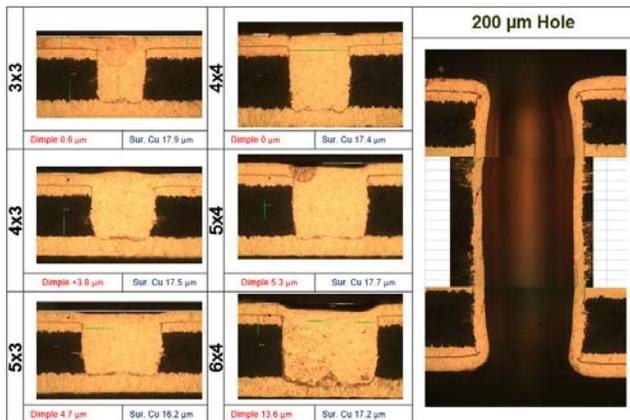


Figure 12: Via and through hole performance of novel formulation at optimum conditions

Physical & Thermal Properties

Tensile strength and elongation % of two separate samples were measured according to the IPC TM-650, 2.4.18.1 standard. One sample was plated when the bath was fresh, at

0 amp*hour/L and the another was plated after the bath was aged for 150 amp*hour/L. The results, shown in Figure 13, far surpass the IPC class III requirements (tensile strength > 36,000 psi, elongation > 18%). The novel formulation is very stable, with negligible change in performance between the initial and aged baths.

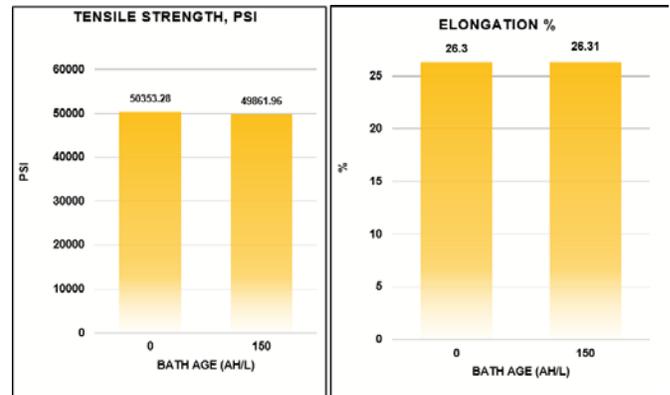


Figure 13: Physical properties of deposited copper when bath was initially made vs. when the bath was aged 150 amp*hour/L.

CONCLUSION

V-pit formation is a significant issue for manufacturers who must etch copper surfaces many times during multilayer build up. The novel formulation we tested deposits Cu that forms significantly fewer pits after etching than incumbent processes. Use of an electrolytic copper formulation that produces V-pitting resistant deposits can help solve the issue of pitting in circuit manufacturing without using time and energy intensive annealing processes. The formulation tested successfully plates multiple features (vias and through holes) with physically robust Cu, which meets the strict requirements of high-density interconnect applications.

During our evaluation process, we investigated the impact of surface contaminations on pit formation. We found that intentionally introducing contaminants on the general surface was correlated to high concentrations of pits forming during the etching step, if conventional formulations were used. When the novel formulation was utilized, the areas with surface contamination did not show subsequent pit formation.

Certain vias contained contamination, detected by SEM/EDS. When these boards were plated and etched, there was preferential pitting on the filled vias, even when utilizing the novel formulation. However, the pitting was far less severe.

The correlation between contaminants being incorporated into the deposited copper and the prevalence of pits in subsequent etching steps that we observed is in agreement with literature (1) (2).

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